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Substitute for form 1449-PTO

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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### Complete if Known

Application Number	09/616385
Filing Date	07/14/00
First Named Inventor	Enric Musoll
Art Unit	2183
Examiner Name	Eric Coleman
Sheet	1 of 3
	Attorney Docket Number
	MIPS.0165-00-US

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
EC		6105127	Kozo et al	08-15-2000	
EC		09/592106	Melvin et al.	filed 06-12-2000	
EC		09/595776	Musoll et al.	filed 06-16-2000	
EC		09/616385	Musoll et al.	filed 07-14-2000	
EC		09/629805	Nemirovsky et al.	filed 07-31-2000	
EC		09/312302	Nemirovsky et al.	filed 05-15-1999	
EC		09/273810	Nemirovsky et al.	filed 03-22-1999	
EC		20020062435	Nemirovsky et al.	05-23-2002	
EC		09/240012	Nemirovsky et al.	filed 01-27-1999	
EC		6356996	Adams, Phillip M.	03-12-2002	
EC		6260077	Rangarajan et al.	07-10-2001	
EC		20030084269	Drysdale et al.	05-01-2003	
EC		6493749	Paxhia et al.	12-10-2002	
EC		6430593	Lindsley, Brett Louis	08-06-2002	
EC		6442675	Derrick et al.	08-27-2002	
EC		6192384	Dally et al.	02-20-2001	
EC		4197579	Forsman et al.	04-08-1980	

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Sheet	2	of	3	Attorney Docket Number	MIPS.0165-00-US

FOREIGN PATENT DOCUMENTS							
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		Country Code <sup>x</sup>	Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
EC	BA	JP	10207717A2 (Translation of Relevant Parts and Abstract provided)	08-07-1998	Matsuzaki et al.		Yes
EC	BB	JP	1011301A2 (Translation of Relevant Parts and Abstract provided)	01-16-1998	Imai et al.		Yes
EC	BC	JP	09506752A2 (Translation of Relevant Parts and Abstract provided)	06-30-1997	Dobbins et al.		Yes
EC	BD	JP	10124316A2 (Translation of Filing Particulars and Abstract provided)	05-15-1998	Kimura et al.		Yes
EC	BE	JP	2103630 (Translation of Relevant Parts and Abstract Provided)	10-12-1988	Makita et al.		Yes
EC	BF	JP	4335431 (Translation of Relevant Parts and Abstract Provided)	11-24-1992	Sakai, Nonaki		Yes
EC	BG	JP	63254530 (Translation of Relevant Parts and Abstract Provided)	10-21-1988	Tanitsu, Eiji		Yes
EC	BH	JP	546379(Translation of Relevant Parts and Abstract Provided)	02-26-1993	Okazaki et al.		Yes
EC	BI	EP	0827071A2	03-04-1998	Kimura et al.		
EC	BJ	WO	9427216A1	11-24-1994	Keckler et al.		
EC	BK	EP	0806730A2	11-12-1997	Zolnowsky, John E.		
EC	BL	WO	00023891A1	04-27-2000	Lundstrom et al.		

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NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T <sup>2</sup>
E.C.	CA	CUI ET AL., Parallel Replacement Mechanism for MultiThread, Advances in Parallel and Distributed Computing, 1997. Proceedings, IEEE, March 21, 1977, pp. 338-344				
E.C.	CB	TULLSEN ET AL., Supporting Fine-Grained Synchronization on a Simultaneous Multithreading Processor, USCD CSE Technical Report CS 98-587, June 1998, all pages, US				
E.C.	CC	THEKKATH ET AL. The Effectiveness of Multiple Hardware Contexts. In Proceedings of the 6th International Conference on Architectural Support for Programming Languages and Operating Systems, pages 328-337, San Jose, CA, October 1994. ACM				
E.C.	CD	MCFARLING, SCOTT. Combining Branch Predictors. WRL Technical Note TN-36. June 1993. Pages 11-12. Digital Western Research Laboratory. Palo Alto, CA, US				

Examiner Signature	<i>Eric Coleman</i>	Date Considered	6/14/05
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(use as many sheets as necessary)				Filing Date	07/14/00
				First Named Inventor	Enrique Musoll Mario D. Nemirovsky
				Group Art Unit	2183
				Examiner Name	Eric Coleman
Sheet	1	of	2	Attorney Docket Number	MIPS.0165-00-US

<b>OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS</b>				
Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
EC	AA	"The PowerPC Architecture: A Specification for a New Family of RISC Processors", Second Edition, May 1994, pp.70-72, Morgan Kaufmann, San Francisco.		T <sup>2</sup>
EC	AB	MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp3-125, 3-126, and 3-127, Prentice Hall, New Jersey		
EC	AC	POTEL, M.J., "Real-time Playback in Animation Systems", Proceedings of the 4 <sup>th</sup> Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp.72-77, San Jose, CA.		
EC	AD	ARM Architecture Reference Manual, 1996, pp.3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall.		
EC	AE	ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at <a href="http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ(AR001/CONTENTS)">http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ(AR001/CONTENTS)</a> )		
EC	AF	MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp.10-66, 10-67, and 10-71, Motorola, Inc.		
EC	AG	DIFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp.40-63, Vol. 12, No.2.		
EC	AH	KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp.7-106 and 7-107, Prentice hall, New Jersey.		
EC	AI	DIEFENDORFF, KEITH et al., "AltiVec Extension to PowerPC Accelerates Media Processing", March -April 2000, pp.85-95, IEEE Micro, Vol. 20, No.2.		
EC	AJ	PAI, VIJAY et al., "An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors", Proceedings of ASPLOS VII, October 1996, pp.12-23, ACM, Inc.		
EC	AK	FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp.210-211, IEEE.		

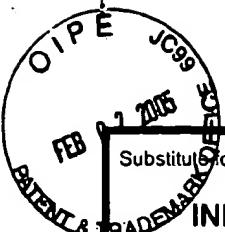
Examiner Signature	<i>Eric C</i>	Date Considered	6/14/05
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(use as many sheets as necessary)				Filing Date	07/14/00
				First Named Inventor	Enrique Musoll Mario D. Nemirovsky
				Group Art Unit	2183
				Examiner Name	Eric Coleman
Sheet	2	of	2	Attorney Docket Number	MIPS.0165-00-US

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
EC	AL	YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of CA, Santa Barbara dissertation, December 1995, Santa Barbara, CA.			T <sup>2</sup>
EC	AM	STEERE et al, "A Feedback-Driven Proportion Allocator for Real Estate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp.145-158, USENIX Association.			
ES	AN	YAMAMOTO, WAYNE, et al., "Increasing Superscalar Performance Through Multistreaming", 1995.			
EC	AO	TULLSEN, DEAN, et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22 <sup>nd</sup> Annual International Symposium on Computer Architecture, June 1995, Santa Margherita, Ligure, Italy.			
EC	AP	YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp.42-53. IEEE.			
EC	AQ	KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of -Order Execution at 600 Mhz", August 1998.			
EC	AR	TULLSEN, et al., "Supporting Fine-Grained synchronization on a Simultaneous Multithreading Processor, UCSD CSE Technical Report CS98-587, June 1998, all pages, US.			
EC	AS	NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998.			
EC	AT	LI et al, "Design and Implementation of a Multiple-Execution-Pipeline Architecture", 7 <sup>th</sup> International Conference on Parallel and Distributed Computing and Systems, October 1995.			
EC	AU	DONALSON et al., "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance", 26 <sup>th</sup> Hawaii Conference on Systems Sciences, 1993, pp. 448-456, volume 1.			
EC	AV	NEMIROVSKY et al., "DISC: Dynamic Instruction Stream Computer ACM, 1991, pp. 163-171.			
EC	AW	YAMAMOTO, WAYNE et al, "Performance Estimation of Multistreamed, Superscalar Processors", IEEE, 1994, pp. 195-204, Hawaii, US			
EC	AX	GRUENWALD, et al., "Towards Extremely Fast Context Switching in a Block-Multithreaded Processor", Proceedings of EUROMICRO – 22, 1996, pp. 592-599			
EC	AY	BRADFORD, JEFFREY et al., "Efficient Synchronization for Multithreaded Processors", Workshop on Multithreaded Execution, Architecture and Compilation, January-February 1998, pp.1-4.			

Examiner Signature	Eric Coleman	Date Considered	6/14/05
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<b>Sheet</b>	1	<b>of</b>	1	<b>Attorney Docket Number</b>	MIPS.0165-00-US

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Examiner Signature	<i>Eve Cok</i>	Date Considered	6/14/05
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Sheet

1

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2

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## **U.S. PATENT DOCUMENTS**

## **FOREIGN PATENT DOCUMENTS**

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